Amendments to the Specification

Please replace the paragraph beginning on page 4, line 14 with the following amended paragraph:

Source regions 65 and 68 [[69]], and drain regions 66 and 69 [[68]] are formed underneath the boundary portion between the gate insulator 64 and the wells 62 and 63.

Please replace the paragraph beginning on page 14, line 12 with the following amended paragraph:

The timing generator circuit 21 is a circuit for applying a power supply voltage, a timing pulse, and so on to the above-described vertical shift resistor 22 and the horizontal shift resistor 23 [[22]].

Please replace the paragraph beginning on page 18, line 23 with the following amended paragraph:

As to the output transistor 2312, the gate is connected with the source region of the charge transistor 2311 via the node 2315 as described above, the drain region is connected with a signal line for the drive pulse V1, and the source region is connected with the other end (the minus terminal) of the bootstrap capacitor 2313. The source region of the output transistor 2312 is connected with the drain region of the discharge transistor 2317 as well.

Please replace the paragraph beginning on page 19, line 21 with the following amended paragraph:

As described above, the horizontal shift resistor 23, whose transistor is formed with only n-channel MOS type, includes four transistors and one capacitor for each stage. The above-described conventional horizontal shift resistor having the conventional CMOS type structure, which is shown in FIG.11, includes 16 transistors for each stage. Meanwhile, the horizontal shift resistor 23 includes fewer functional device units (transistors and a capacitor), namely only five in total.

Please replace the paragraph beginning on page 20, line 14 with the following amended paragraph:

As FIG.4 shows, in the horizontal shift resistor 23, the charging transistor 2311 is turned on when a start pulse VST (voltage 5(V)) is applied to the gate electrode of the charging transistor 2311 at a time t0. When the charging transistor 2311 is turned on, a voltage begins to be applied to the gate electrode of the output transistor 2312, and the output transistor 2312 is turned on as well. Here, the drive pulse V1, which is input to the drain region of the output transistor 2312, is a ground potential, and a potential difference, which is the same as the power supply voltage VDD, occurs between the both ends of the bootstrap capacitor 2313. As a result, the bootstrap capacitor 2313 is to be charged until it gains the same voltages as the power supply voltage VDD (3(V)).

Please replace the paragraph beginning on page 24, line 8 with the following amended paragraph:

The following describes a method for forming the transistor included in the MOS type imaging apparatus 1, with reference to FIGs. 6A through 6D and FIGs 7A and 7B ~~FIG.6 and FIG.7~~.

Please replace the paragraph beginning on page 24, line 14 with the following amended paragraph:

By depositing polysilicon (polycrystalline silicon) in a predetermined area on the surface of the gate insulator 32, a gate electrode 35 is formed as shown in FIG. 6C ~~FIG.6~~. For forming the gate electrode 35, the LPCVD method may be used, for instance.